Claims:

1. A method for enabling scan test vectors to be generated by an automatic test vector generating software program for a customer designed integrated circuit having an embedded vendor circuit which includes a proprietary circuit and a nonproprietary circuit and which also includes customer supplied circuitry, comprising:

creating at least one pseudo input to represent at least a portion of said nonproprietary circuit that is not necessary to be exercised by said automatic test vector generating software program to generate test vectors for said customer designed integrated circuit;

identifying an output node of said embedded vendor circuit to which an input of said customer designed circuit is connectable; and

creating a test netlist which represents circuitry that produces output states at said output node which would be generated by said embedded vendor circuit thereat; said test netlist including said at least one pseudo input and said output node, without including a full netlist of either said proprietary or nonproprietary circuits;

whereby scan test vectors for the customer designed integrated circuit can be generated by said automatic test vector generating software program using said test netlist with said output node connected to an input of a netlist representing said customer supplied circuitry.

2. The method of claim 1 wherein said at least one pseudo input is a pseudo pin in said test netlist.

3. The method of claim 1 wherein said automatic test vector generating software program is an ATPG software program which generates test vectors by using said test netlist.

4. The method of claim 1 wherein said embedded vendor circuit includes a proprietary DSP circuit and a nonproprietary JTAG Interface circuit.

5. A method for generating test vectors to test an integrated circuit having an embedded vendor circuit which includes a proprietary circuit and a nonproprietary circuit and which also includes customer supplied circuitry, comprising:

creating at least one pseudo input to represent at least a portion of said nonproprietary circuit that is intended to emulate said nonproprietary circuit output to generate test vectors at least for said customer supplied circuitry;

identifying an output node of said embedded vendor circuit to which an input of said customer supplied circuitry is connectable;

creating a test netlist which represents circuitry that produces output states at said output node which would be generated by said embedded vendor circuit thereat; said test netlist including said at least one pseudo input and said output node, without including a full netlist of either said proprietary or nonproprietary circuits;

combining a netlist of said customer supplied circuitry with said test netlist to form a total netlist;

applying an automatic test vector generating software program to said total netlist to generate test vectors therefor.

6. The method of claim 5 wherein said at least one pseudo input is a pseudo pin in said test netlist.

7. The method of claim 5 wherein said automatic test vector generating software program is an ATPG software program which generates test vectors by using said test netlist.

8. The method of claim 5 wherein said embedded vendor circuit includes a proprietary DSP circuit and a nonproprietary JTAG Interface circuit.

9. The method of claim 5 further comprising stripping references to said at least one pseudo input from said total netlist.

10. The method of claim 9 further comprising applying the generated test vectors to said total netlist from which the at least one pseudo input has been stripped.

11. A system for generating a test netlist of an embedded vendor circuit which includes a proprietary circuit and a nonproprietary circuit for use by a customer in adding thereto customer supplied circuitry, comprising:

means for creating a test netlist which represents circuitry having at least one pseudo input to represent at least a portion of said nonproprietary circuit that is not necessary to be exercised by an automatic test vector generating software program;

whereby when a netlist for said customer supplied circuitry is combined with said test netlist, scan test vectors at least for said customer supplied circuitry can

be generated by an automatic test vector generating software program.

12. The system of claim 11 wherein said at least one pseudo input is a pseudo pin in said test netlist.

13. The system of claim 11 wherein said automatic test vector generating software program is an ATPG software program which generates test vectors.

14. The system of claim 11 wherein said embedded vendor circuit includes a proprietary DSP circuit and a nonproprietary JTAG Interface circuit.